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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,067	07/03/2003	Glen J. Leedy	ELM-2 DIV . 6	8117

1473 7590 09/21/2005

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,067	LEEDY, GLEN J.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-165* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *88-145* is/are allowed.

6)☒ Claim(s) *146-148,150-154,156-158 and 160-164* is/are rejected.

7)☒ Claim(s) *149,155,159 and 165* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28, 8/10, 9/6/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *8/9/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the RCE on 28 June 2005. Claims 88-165 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 146, 150-154, 156 and 160-164 are rejected under 35 U.S.C. 102(b) as being anticipated by Faris (5,786,629).

Referring to claims 146 and 156, Faris discloses an integrated circuit structure including a plurality of semiconductor dice (2), each die having an integrated circuit (6) formed thereon, the dice (2) being stacked in layers, wherein at least one of the plurality of dice is substantially flexible; and between adjacent dice, a bonding layer (17) bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice (Fig. 4; col. 6, lines 12-27; col. 7, lines 1-12; col. 8, lines 1-7).

Referring to claims 150 and 162, Faris discloses wherein at least one of the plurality of dice has a substrate, wherein at least one of a major portion of the substrate is removed and a major portion of the substrate is able to be removed while retaining

the structural integrity of the integrated circuit formed on the substrate (col. 6, lines 12-27).

Referring to claim 151, Faris discloses wherein at least one of the pluralities of dice a substantially rigid substrate having a first thickness (col. 6, lines 12-27).

Referring to claim 152, Faris discloses wherein at least one of the plurality of dice has a second thickness, wherein the second thickness is substantially less than the first thickness (col. 6, lines 12-27).

Referring to claims 153 and 163, Faris discloses forming at least one of interconnects between adjacent bonded surfaces of adjacent dice and wire interconnects formed between the dice (col. 5, lines 15-22; col. 7, lines 31-44).

Referring to claims 154 and 164, Faris discloses performing information processing on data routed between any two of the plurality of dice (col. 4, lines 51-65).

Referring to claim 160, Faris discloses the substrate having circuitry formed thereon (col. 7, lines 45-67).

Referring to claim 161. (Previously presented) The apparatus of claim 156, wherein the substrate is formed from a non-semiconductor material (col. 3, lines 29-38).
162. (Previously presented) The apparatus of claim 156, wherein the die has a substrate, wherein at least one of a major portion of the substrate of the die is removed and a major portion of the die is able to be removed while retaining the structural integrity of the integrated circuit formed on the die.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 147, 148 157 and 158 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faris in view of Wojnarowski (5,324,687).

Faris discloses the subject matter claimed above except at least one of the pluralities of integrated circuit substrates is formed with a low stress dielectric.

Wojnarowski discloses circuitry comprising a plurality of substrates (10, 30) having integrated circuits (12, 14) formed thereon (Fig. 3; col. 5, lines 25- 53), wherein at least one of the plurality of substrates is a substantially flexible substrate (Fig. 7; col. 8, lines 10-38); and between adjacent substrates (10, 30), a bonding layer (28) bonding together the adjacent substrates (10, 30), the bonding layer (28) being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof (Fig. 3; col. 5, lines 36-66).

Referring to claims 147 and 157, Wojnarowski discloses at least one of the pluralities of integrated circuit substrates is formed with a low stress dielectric (Fig. 1; col. 4, lines 12-38).

Since Faris and Wojnarowski are both from the same field of endeavor, an integrated circuit device, the purpose disclosed by Wojnarowski would have been recognized in the pertinent art of Faris. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Faris by at least one of the plurality of integrated circuit substrates is formed with a low stress dielectric as taught by Wojnarowski to product flexible circuit packages or modules (col. 1, lines 62-65).

Referring to claims 148 and 158, Faris does not disclose the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less. It would have been obvious to one having ordinary skill in the art at the time invention was made to have the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Allowable Subject Matter

Claims 149, 155, 159 and 165 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest the stress of the low stress dielectric is tensile; and at least one of the substrate and die having at least one of

polycrystalline active circuitry formed thereon, die has reconfiguration circuitry formed thereon and passive circuitry formed thereon.

Claims 88-145 are allowed.

The following is an examiner's statement of reasons for allowance: referring to claim 88, prior art does not anticipate, teach, or suggest circuitry where a plurality of monolithic substrates have integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate; and between adjacent substrates, a bonding layer bonding together the adjacent substrates, the bonding layer being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof.

Referring to claim 97, prior art does not anticipate, teach or suggest an integrated circuit structure where a first substrate has a first surface; and a second substrate bonded to the first surface of the first substrate to form conductive paths between the first substrate and the second substrate wherein the second substrate is a substantially flexible monolithic monocrystalline semiconductor substrate having active circuitry formed thereon, wherein no other substrates are bonded to the first surface.

Referring to claim 101, prior art does not anticipate, teach or suggest a stacked integrated circuit where a plurality of integrated circuit substrates have formed on corresponding surfaces thereof complementary patterns of a material bondable using thermal diffusion bonding, wherein at least one of the plurality of substrates is a

substantially flexible monolithic integrated circuit substrate; and a thermal diffusion bonded region between the complementary patterns.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Clifton (RE37,673), Clifton et al. (5,480,842) and Flesher et al. (5,733,814) all disclose flexible circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP